REMARKS/DISCUSSION OF ISSUES

By this Amendment, Applicant amends claims 1-3, 5-8 and 10, cancels claim 9 without prejudice against future prosecution or disclaimer of the underlying subject matter, and adds new claim 11. Accordingly, claims 1-8 and 10-11 are pending in the application.

Applicant thanks the Examiner for acknowledging the claim for priority and receipt of certified copies of all the priority documents, and for indicating that the drawings are acceptable.

Reexamination and reconsideration are respectfully requested in view of the following remarks.

OBJECTION TO THE SPECIFICATION

Applicant thanks the Examiner for providing information about recommended section headings. However, Applicant respectfully declines to add the headings. Section headings are not statutorily required for filing a non-provisional patent application under 35 USC § 111(a), but per 37 CFR § 1.51(d) are only guidelines that are suggested for applicant's use. (See Miscellaneous Changes in Patent Practice, Response to comments 17 and 18 (Official Gazette, August 13, 1996) [Docket No: 950620162-6014-02] RIN 0651-AA75 ("*Section 1.77 is permissive rather than mandatory. ... [T]he Office will not require any application to comply with the format set forth in 1.77*")).

Accordingly, Applicant respectfully request that the objection to the specification be withdrawn.

CLAIM OBJECTIONS

The Office Action objects to claims 1-2, 5-6 and 8 on various grounds.

Applicant has amended claims 1-2, 5-6 and 8 and respectfully submits that the claim amendments overcome the claim objections.

Accordingly, Applicant respectfully requests that the objections to claims 1-2, 5-6 and 8 be withdrawn.

35 U.S.C. § 112

The Office Action rejects claims 1-8 and 10 under 35 U.S.C. § 112.

Applicant has amended claims 1 and 5 and respectfully submits that the claim amendments overcome the rejections under 35 U.S.C. § 112.

Accordingly, Applicant respectfully requests that the rejections of claims 1-8 and 10 under 35 U.S.C. § 112 be withdrawn.

35 U.S.C. § 102 & 103

The Office Action rejects claims 1, 3, 4-6, 8 and 10 under 35 U.S.C. § 102 over Cohen EP0690370 ("Cohen"), and claims 2 and 7 under 35 U.S.C. § 103 over Cohen in view of Delvaux et al. U.S. Patent 6,851,046 ("Delvaux").

Applicant respectfully traverses these rejections for at least the following reasons.

Claim 1

Among other things, the microcontroller of claim 1 is adapted to execute a conditional branch instruction, wherein in case of a fulfilled branch condition at least one program counter is loaded with a new address or a new value, and in case of an unfulfilled branch condition the instruction is optionally either ended immediately, or the at least one program counter is reloaded with its current address or current value prior to ending the instruction.

Applicant respectfully submits that Cohen does not disclose any microprocessor including such a combination of features.

The Office Action cites page 8, line 41 – page 9, line 29, describing operation of the "jump unit" shown in FIG. 7 of Cohen.

However, the cited text does not describe any feature wherein in case of an unfulfilled branch condition the instruction is ***optionally*** either ended immediately, ***or the program counter is reloaded with its current address or current value prior to ending the instruction***.

The Office Action states that "*any instruction's execution, including that of a*

conditional branch, would result in a new address being loaded into the program counter if even to simply increment the program counter upon the completion of the current instruction."

Applicant respectfully disagrees. ***Incrementing*** a counter is not the same as ***loading*** the counter register with a new address. In general, during a program cycle of a microcontroller, a program counter's value is automatically incremented when the current instruction is being performed, so that at the end of the instruction, the program counter automatically points to the next instruction to be performed. However, whenever a branch occurs, then a new address has to be loaded into the counter. This loading operation consumes a certain amount of time that is not required for automatic incrementation of the counter value. In the prior art, this causes a time difference for execution of the next instruction between: (a) a first case where no branch occurs and the address in the program counter is merely automatically incremented; and (b) a second case where a branch occurs and the branch address must be loaded into the program counter. Anyone of skill in the art who understands how a counter operates would clearly understand this principle.

In contrast, in the microcontroller of claim 1, optionally even when no branch occurs, program counter is reloaded with its current address prior to ending the instruction.

So, Applicant respectfully disagrees with the statement in the Office Action that any instruction's execution in Cohen would result in a new address being loaded into the program counter. Therefore, for at least these reasons, Applicant respectfully submits that Cohen does not disclose or suggest any microcontroller wherein in case of an unfulfilled branch condition the instruction is optionally either ended immediately, or the program counter is reloaded with its current address or current value prior to ending the instruction.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 1 is patentable over Cohen.

Claims 3-4

Claims 3-4 depend from claim 1 and are deemed patentable for at least the

reasons set forth above with respect to claim 1. Applicant also specifically traverses the statement in the Office Action that a microcontroller is inherently a smartcard.

Claim 5

Among other things, the method of claim 1 includes comprising executing a conditional branch instruction, wherein in case of a fulfilled branch condition at least one program counter is loaded with a new address or a new value, and in case of an unfulfilled branch condition the instruction is optionally either ended immediately, or the at least one program counter is reloaded with its current address or current value prior to ending the instruction.

As explained above with respect to claim 1, Applicant respectfully submits that Cohen does not disclose such a combination of features.

Accordingly, for at least these reasons, Applicant respectfully submits that claim 5 is patentable over Cohen.

Claims 6, 8 and 10

Claims 6, 8 and 10 depend from claim 5 and are deemed patentable for at least the reasons set forth above with respect to claim 5. Applicant also specifically traverses the statement in the Office Action that the recited special bit is inherently present in Cohen's robust jump instruction, for a variety of reasons, including the failure of Cohen to disclose that its apparatus of FIG. 7 supports both the robust jump instruction and a so-called "regular jump instruction" mentioned (without any citation) in the Office Action. Also, in any event the robust jump instruction pertains to a mechanism to verify the integrity of the instruction, and to ***jump to an address for an error routine*** when the integrity of the instruction has been compromised. This has nothing to do with determining whether to end an instruction immediately, or to reload a program counter with its current address or current value prior to ending the instruction, which is controlled by the recited special bit.

NEW CLAIM 11

Among other things, the microcontroller of claim 11 the microcontroller includes a program counter and a multiplexer, wherein in case of a fulfilled branch

condition the multiplexer is controlled to load the branch address into the program counter, and wherein in case of an unfulfilled branch condition the multiplexer is controlled to reload the program counter with its current address prior to ending the instruction. In particular, no combination of the prior art remotely suggests that, in case of an unfulfilled branch condition, a multiplexer is controlled to reload the program counter with its current address prior to ending the instruction.

Accordingly, Applicant respectfully submits that claim 11 is clearly patentable over the cited prior art.

CONCLUSION

In view of the foregoing explanations, Applicant respectfully requests that the Examiner reconsider and reexamine the present application, allow claims 1-8 and 10-11 and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283.0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this reply to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

VOLENTINE & WHITT

Date: 20 March 2007

By: _____
Kenneth D. Springer
Registration No. 39,843

VOLENTINE & WHITT
11951 Freedom Drive, Suite 1260
Reston, Virginia 20190
Telephone No.: (571) 283.0724
Facsimile No.: (571) 283.0740